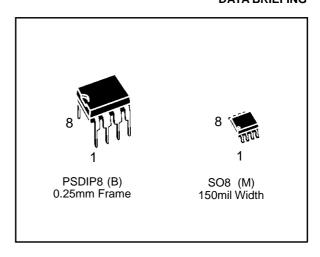


# SERIAL ACCESS SPI BUS 2K (256 x 8) EEPROM

#### **DATA BRIEFING**

- 100,000 ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- SINGLE 4.5V to 5.5V SUPPLY VOLTAGE
- SPI BUS COMPATIBLE SERIAL INTERFACE
- 2 MHz CLOCK RATE MAX
- BLOCK WRITE PROTECTION
- STATUS REGISTER
- 16 BYTE PAGE MODE
- WRITE PROTECT
- SELF-TIMED PROGRAMMING CYCLE
- E.S.D.PROTECTION GREATER than 4000V
- SUPPORTS POSITIVE CLOCK SPI MODES (ST95020)
- SUPPORTS NEGATIVE CLOCK SPI MODES (ST95021)



## **DESCRIPTION**

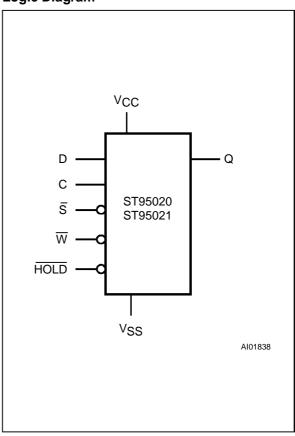
The ST95020 and ST95021 are 2K bit Electrically Erasable Programmable Memories (EEPROM) fabricated with SGS-THOMSON's High Endurance Single Polysilicon CMOS technology. The memory is accessed by a simple SPI bus compatible serial interface. The bus signals are a serial clock input (C), a serial data input (D) and a serial data output (Q).

The device connected to the bus is selected when the chip select input  $(\overline{S})$  goes low. Communications with the chip can be interrupted with a hold input  $(\overline{HOLD})$ . The write operation is disabled by a write protect input  $(\overline{W})$ .

For the ST95020, data is clocked in during the low to high transition of clock C, data is clocked out during the high to low transition of clock C.

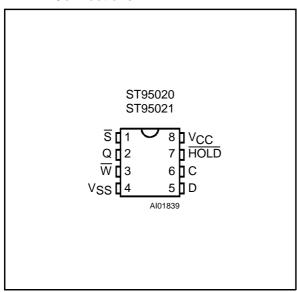
For the ST95021, data is clocked in during the high to low transition of clock C, data is clocked out during the low to high transition of clock C.

#### **Logic Diagram**

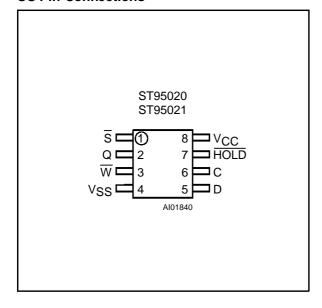


B95020/606 1/2

#### **DIP Pin Connections**



### **SO Pin Connections**

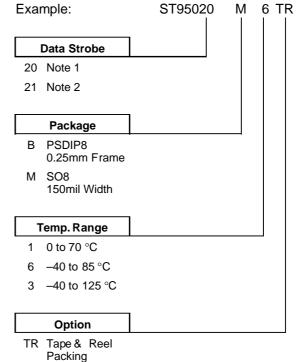


### **Signal Names**

С	Serial Clock
D	Serial Data Input
Q	Serial Data Output
S	Chip Select
W	Write Protect
HOLD	Hold
Vcc	Supply Voltage
V <sub>SS</sub>	Ground

**Ordering Information Scheme**For a list of available options refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact the SGS-THOMSON Sales Office nearest to you.



- Notes: 1. Data In is strobed on rising edge of the clock (C) and Data Out is synchronized from the falling edge of the
  - Data In is strobed on falling edge of the clock (C) and Data Out is synchronized from the rising edge of the clock.